REMARKS

Claims 1-19 of the present application remain pending. Claims 17, 18, and 19 are amended herein. Applicants respectfully submit that no new matter is added as a result of the claim amendments.

CLAIM OBJECTIONS

Claims 17 and 18 are objected to for informalities. Claims 17 and 18 are amended herein to depend on independent Claim 16. Accordingly, the Applicants respectfully request withdrawal of the claim objections.

CLAIM REJECTIONS 35 U.S.C. § 102

Claims 1-19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kobayashi et al (U.S. Patent No. 6,199,091), hereinafter referred to as "Kobayashi." The Applicants respectfully submit that these claimed embodiments of the present invention are not anticipated or suggested by Kobayashi. Claim 1 of the present invention is directed to a method of performing a pipelined arithmetic function and recites (emphasis added):

> a) receiving two N-bit operands into each of a plurality of adder elements in separate pipelines;

b) performing an add operation in each of said plurality of adder elements wherein a first N-bit result and a first carry bit is output from each of said adder elements;

c) receiving said first N-bit result from each of said adder elements into a respective N-bit result register and receiving said first carry bit from each of said adder elements into a respective carry bit register;

d) outputting from an incrementor in one of said pipelines, a second N-bit result and a second carry bit from the combination of a first result from a first of said N-bit result registers, a first carry bit from a first of said carry bit registers, and a first carry bit from a second of said carry bit registers from a second of said pipelines; and

e) supplying a final result being a combination of said second N-bit result from said incrementor, said second carry bit from said incrementor, and said first N-bit result from a second N-bit result register in said second pipeline.

The embodiments of Claims 8 and 16 are directed to a pipelined adder/subtractor and a multistage adder/subtractor respectively and recite similar claim limitations. The Applicants respectfully submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

a) receiving two N-bit operands into each of a plurality of adder elements in separate pipelines;

The embodiments of Kobayashi teach that the N-bit operand is not received into each of the separate pipelines. Instead, portions of each of the two N-bit operands (e.g., X0-X26 and Y0-Y26 of Figures 1 and 2) are distributed among the separate combinatorial pathways. Thus, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching Kobayashi which distributes portions of the N-

bit operands among the pathways and that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants further submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

> b) performing an add operation in each of said plurality of adder elements wherein a first N-bit result and a first carry bit is output from each of said adder elements;

For example, the rejection cites the Z0-Z2 as comprising a first pipeline and Z3-Z8 as comprising a second pipeline. In the embodiment of Figures 1 and 2 of Kobayashi, X and Y are both 27 bit operands, thus, N=27. However, while the apparatus of Kobayshi receives a 27 bit operand, the first pipeline only outputs a 3 bit result, the second pipeline outputs a 6 bit result, the third pipeline outputs a 7 bit operand, and the fourth pipeline outputs an 11 bit operand. Thus, the Applicants respectfully submit that Kobayashi teaches away from embodiments of the present invention which recite that each of the adder elements in each pipeline receives two N-bit operands and outputs an N-bit result. Accordingly, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching of Kobayashi which does not output an N-bit result from each of the adder elements and that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants further submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

> c) receiving said first N-bit result from each of said adder elements into a respective N-bit result register and receiving said first carry bit from each of said adder elements into a respective carry bit register;

The rejection states the existence of registers to store the results for Z0-Z2. However, Kobayashi does not specifically teach or suggest storing the results of Z0-Z2 in a register whose contents are used in another pipeline. Furthermore, Kobayashi does not teach or suggest that the results from the other adder elements (e.g., Z3-Z8, Z9-Z15, Z16-Z22, and Z23-Z26) are stored in a result register. Nor does Kobayashi teach or suggest the recited claim limitation of receiving said first carry bit from each of said adder elements into a respective carry bit register. Instead, the carry bits of the apparatus shown by Kobayashi (e.g., C1, C3, and C4) are direct inputs into the other pathways without a register. Thus, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching Kobayashi which does not store an N-bit result from each adder element in a respective N-bit register and which does not receive a carry bit from each of the adder elements into a respective carry bit register. Therefore, the Applicants respectfully submit that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants assert that Kobayashi does not teach result registers and carry bit registers because Kobayashi's design is not pipelined, as claimed. for instance, Kobayashi does not teach use of clocked pipestages within a pipeline where the results of one clocked pipeline are fed to a downstream pipestage via clocked registers. Kobayashi's circuit is merely one combinatorial circuit pathway that is not clocked, therefore it does not require result registers and it does not require carry bit registers and therefore these elements, as claimed in the present invention, are not taught nor suggested by Kobayashi.

The Applicants respectfully submit that Kobayashi does not teach or suggest the recited claim limitation of (emphasis added):

> d) outputting from an incrementor in one of said pipelines, a second N-bit result and a second carry bit from the combination of a first result from a first of said N-bit result registers, a first carry bit from a first of said carry bit registers, and a first carry bit from a second of said carry bit registers from a second of said pipelines;

The Applicants respectfully submit that Kobayashi does not teach or suggest an incrementor of any sort. While the rejection cites the all the logics in the lower portion of the pipeline producing Z3-Z4 except 7 and 9 as comprising an incrementor, Kobayashi does not teach or suggest that the function of an incrementor is performed by these logic elements or other elements shown in Figures 1-4. Thus, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching

Kobayashi which does not teach or suggest an N-bit result from an incrementor and that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants respectfully submit that the embodiments of the present invention recited in Claims 1 and 8 recite a pipelined arithmetic function and a pipelined adder/subtractor respectively. Claim 17 recites a plurality of pipelines, each of which is divided into clock regulated pipestages. The Applicants respectfully submit that it is well known by one skilled in the relevant art that a pipelined arithmetic function and a pipelined adder/subtractor also refer to an implementation which utilizes clock regulated pipestages. The Applicants respectfully submit that Kobayashi does not teach or suggest that clock regulated stages are used in any manner. Instead, the combinatorial adders and associated logic shown by Kobayashi perform their functions in a single clock cycle. Accordingly, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not taught or suggested by Kobayashi and that the rejections under 35 U.S.C. § 102(e) are overcome.

Claims 2-7 depend from Claim 1 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the rejections of Claims 2-7 under 35 U.S.C. § 102(e) are overcome.

Claims 9-15 depend from Claim 8 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the rejections of Claims 9-15 under 35 U.S.C. § 102(e) are overcome.

Claims 17-19 depend from Claim 16 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the rejections of Claims 17-19 under 35 U.S.C. § 102(e) are overcome.

CONCLUSION

Based on the arguments presented above, the Applicants respectfully assert that Claims 1-19 overcome the rejections of record and, therefore, the Applicants respectfully solicit allowance of these Claims.

The Applicants have reviewed the references cited but not relied upon. The Applicants did not find these references to teach or suggest the present claimed invention: U.S 5,619,441, U.S. 5,636,157, U.S. 6,591,286.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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